

Features

VLSI Brochure

Professional and Experience Faculty

Recoded Session for revision

Hands on experience on EDA tools

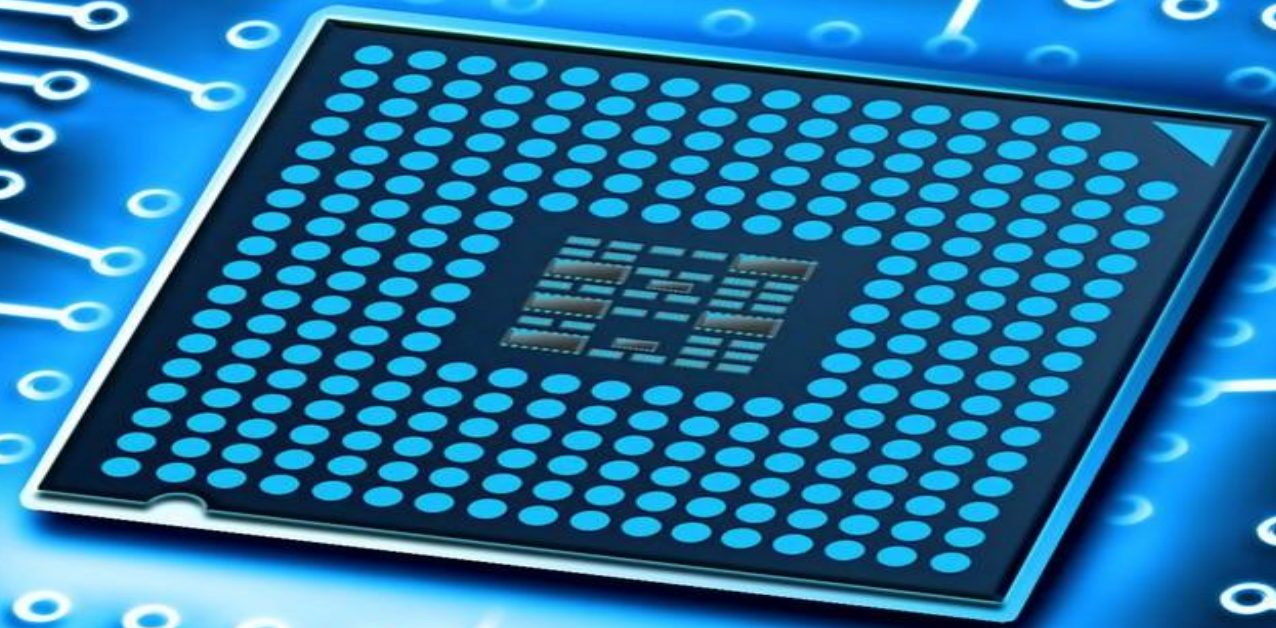
Advance verification methodology

Industrial standards projects

Limited Seats to Give More Personalized Attention

Expert Talk From Industrial Experts

Knowledge Sharing Session



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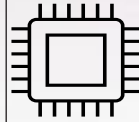
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MODULE 1

Introduction to VLSI

- * what is VLSI ?
- * Introduction
- * VLSI Design Flow
- * Scope
- * Opportunities



MODULE 2

Digital Electronics

- * Digital number system
- * Logic Gates
- * Logic Minimization
- * Combinational Circuit
- * Sequential Circuit
- * Finite State Machine
- * Memories

MODULE 4

UNIX Basic

- * Introduction
- * Handling directory Operation from Command Prompt
- * Handling files Operation from Command Prompt
- * Handling File Editor Application (vi, vim, gvim)

MODULE 6

FPGA, ASIC, SOC

- * Introduction
- * What is FPGA ?
- * What is ASIC ?
- * What is SOC ?
- * Comparison Between FPGA, ASIC, SOC

MODULE 8

System Verilog

- * Introduction
- * System Verilog Data types
- * Arrays In SV
- * Task & Function In SV
- * Interface
- * OOPS & Advance OOPs Concept
- * Randomization & macros
- * Threads, Mailbox, Semaphore, Events
- * System Verilog TB Environment
- * Function Coverage

MODULE 9

System Verilog Assertions

- * Introduction
- * Immediate assertion
- * Simple assertion
- * Sequence composition
- * ABV
- * Assertion Coverage

MODULE 11

Python Scripts

- * Introduction
- * Variable Types
- * Operators
- * number, string and list
- * If else and loops
- * tuple and dictionary
- * Function
- * File I/O Operation

MODULE 13

Industrial Standard Project

- * Specification
- * Design Architecture
- * RTL Design using verilog HDL
- * RTL Verification using system verilog/UVM
- * AXI4/ AXI3/ AHB/ APB/ ASB/ Bridge
- * SPI/ I2C/ UART
- * And many more.....

MODULE 10

UVM Methodology

- * Introduction
- * UVM Factory
- * UVM phases
- * UVM Reporting Mechanism
- * TLM & configuration
- * UVM Sequence
- * UVM TB Environments & Callbacks
- * UVM hack and tricks, report server
- * UVM events, barrier and heartbeats

MODULE 12

The Verification Talk

- * The Verification Plan
- * Testcase strategy
- * What is VIP?
- * How to write a Transaction class?
- * How to write a verification component?
- * The Debugging

MODULE 14

Mini Projects

- * Verilog based mini project
- * System Verilog based mini project
- * UVM based mini project